**SIRIUS FT TEST PLAN GUIDE (ANALOG PART)**

# Revision History

|  |  |  |  |
| --- | --- | --- | --- |
| Version | Date | Author | Note |
| V0.1 | 2017/09/13 | Yuan.yuan,  Zhe.li | Initial version. |
| V0.2 | 2017/09/20 | Yuan.yuan,  Zhe.li | Fill in SPI configure setting for each IP. |

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## Analog FT plan related pins description

Please refer to **Arotsyn\_19x19\_684ballmap.xls** for detailed Pin Number.

For analog related pin description, please refer to the table 1:

TABLE 1 Sirius Analog part pins description

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Sirius analog part pin description, total pin number=25 | | | | |
| Pin Number | IN/OUT | Ball Name | Description | Pad name |
| A24 | IN | XTAL1 | Crystal pad1, or clock input pad, 20M clk input | XTAL1 |
| B24 | OUT | XTAL2 | Crystal pad2. | XTAL2 |
| F20 | IN | CLKREF\_SEL\_PAD | External clock frequency select 0:40MHz,1:20MHz | CLKREF\_SEL\_PAD |
| H20, H21 | IN | AVSS\_A | ABB analog ground | AVSS |
| J20, J21 | IN | AVDD1V8\_A | ABB analog 1.8V supply | AVDD |
| G19 | IN | AVDD1V8\_OSC | Crystal analog 1.8V power | AVDD\_OSC |
| G20 | IN | AVSS\_OSC | Crystal analog ground | AVSS\_OSC |
| K21 | IN | AVDD1V8\_PLL | ABB PLL analog 1.8V power | AVDD\_PLL |
| K20 | IN | AVSS\_PLL | ABB PLL analog ground | AVSS\_PLL |
| E23 | IN | AD\_IN\_0 | SAR3 input analog signal path 0 | SAR10\_IN\_3[0] |
| E22 | IN | AD\_IN\_1 | SAR3 input analog signal path 1 | SAR10\_IN\_3[1] |
| G21 | IN | AD\_IN\_2 | SAR3 input analog signal path 2 | SAR10\_IN\_3[2] |
| E21 | IN | AD\_IN\_3 | SAR3 input analog signal path 3 | SAR10\_IN\_3[3] |
| F21 | IN | AD\_IN\_4 | SAR3 input analog signal path 4 | SAR10\_IN\_3[4] |
| D21 | IN | AD\_IN\_5 | SAR3 input analog signal path 5 | SAR10\_IN\_3[5] |
| D20 | IN | AD\_IN\_6 | SAR3 input analog signal path 6 | SAR10\_IN\_3[6] |
| C20 | IN | AD\_IN\_7 | SAR3 input analog signal path 7 | SAR10\_IN\_3[7] |
| D26 | IN | RSSI\_1 | A channel RSSI input | SAR10\_IN\_1[0] |
| C25 | IN | PDET\_A\_2G | A channel power detector for 2G carrier | SAR10\_IN\_1[1] |
| D24 | IN | PDET\_B\_2G | A channel power detector for 2G carrier | SAR10\_IN\_1[2] |
| C23 | IN | RSSI\_2 | B channel RSSI input | SAR10\_IN\_2[0] |
| C24 | IN | PDET\_A\_5G | A channel power detector for 5G carrier | SAR10\_IN\_2[1] |
| D23 | IN | PDET\_B\_5G | A channel power detector for 5G carrier | SAR10\_IN\_2[2] |
| A25 | OUT | QDAC\_OUTN\_A | QDAC negative output path A | QDAC\_OUTN\_A |
| B25 | OUT | QDAC\_OUTP\_A | QDAC positive output path A | QDAC\_OUTP\_A |
| B26 | OUT | IDAC\_OUTP\_A | IDAC positive output path A | IDAC\_OUTP\_A |
| A26 | OUT | IDAC\_OUTN\_A | IDAC negative output path A | IDAC\_OUTN\_A |
| A27 | IN | IADC\_VINN\_A | IADC negative input path A | IADC\_VINN\_A |
| C26 | IN | IADC\_VINP\_A | IADC positive input path A | IADC\_VINP\_A |
| B27 | IN | QADC\_VINP\_A | QADC positive input path A | QADC\_VINP\_A |
| B28 | IN | QADC\_VINN\_A | QADC negative input path A | QADC\_VINN\_A |
| C28 | IN | QADC\_VINN\_B | QADC negative input path B | QADC\_VINN\_B |
| C27 | IN | QADC\_VINP\_B | QADC positive input path B | QADC\_VINP\_B |
| D27 | IN | IADC\_VINP\_B | IADC positive input path B | IADC\_VINP\_B |
| D28 | IN | IADC\_VINN\_B | IADC negative input path B | IADC\_VINN\_B |
| E28 | OUT | IDAC\_OUTN\_B | IDAC negative output path B | IDAC\_OUTN\_B |
| E27 | OUT | IDAC\_OUTP\_B | IDAC positive output path B | IDAC\_OUTP\_B |
| F27 | OUT | QDAC\_OUTP\_B | QDAC positive output path B | QDAC\_OUTP\_B |
| F28 | OUT | QDAC\_OUTN\_B | QDAC negative output path B | QDAC\_OUTN\_B |
| E26 | IN | IADC\_VINN\_C | IADC negative input path C | IADC\_VINN\_C |
| E25 | IN | IADC\_VINP\_C | IADC positive input path C | IADC\_VINP\_C |
| F25 | IN | QADC\_VINP\_C | QADC positive input path C | QADC\_VINP\_C |
| F26 | IN | QADC\_VINN\_C | QADC negative input path C | QADC\_VINN\_C |
| F27 | IN | QADC\_VINN\_D | QADC negative input path D | QADC\_VINN\_D |
| H27 | IN | QADC\_VINP\_D | QADC positive input path D | QADC\_VINP\_D |
| G27 | IN | IADC\_VINP\_D | IADC positive input path D | IADC\_VINP\_D |
| G28 | IN | IADC\_VINN\_D | IADC negative input path D | IADC\_VINN\_D |
| G13 | IN | CA7\_AVDD1V8 | A7 PLL analog 1.8V power | A7\_AVDD |
| H13 | IN | CA7\_AVSS1V8 | A7 PLL analog ground | A7\_AVSS |
| AB13 | IN | CEVA\_AVDD1V8 | CEVA PLL analog 1.8V power | CEVA\_AVDD |
| AB14 | IN | CA7\_AVSS1V8 | CEVA PLL analog ground | CEVA\_AVSS |
| G12 | IN | DDR\_AVDD1V8 | DDR PLL analog 1.8V power | DDR\_AVDD18 |
| H12 | IN | DDR\_AVSS1V8 | DDR PLL analog ground | DDR\_AVSS |

### SPI Configuration Guide

**Global SPI setting… TBD**

## Analog IP FT load board requirements

The analog related tests include:

1. Analog voltage test.

2. PLL frequency test.

3. DACs (4 identical DACs) test.

4. ADCs (total 11 ADCs, with 8 identical and 3 other ADCs) test.

5. Temperature Sensor (TS) test.

6. PVT Sensor test.

The analog input signal frequency is less than 10M, output signal frequency is less than 5M, clock frequency is less than 50M.

The DAC-ADC loop tests need relay and spectrum. The DACs test also need spectrum to perform FFT, whose accuracy is higher than 62dB.

The TS test requires one commercial TS sensor each site to provide reference temperature. TS test results will store into OTP (One Time Program).

1. Analog DC voltage test.

### Analog DC voltage test requirement

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Analog DC voltage/current need to be tested | | | | | |
| Pin Number | Pin Name | Signal Name | Value | Tolerance (%) | SPI configuration |
| D21 | AD\_IN\_5 | VBG | 1.25V | 10 | 1.2.1 |
| PMU\_IOUT | 40uA | 1.2.2 |
| AVDDL\_LDO | 0.9V | 1.2.3 |
| OSC\_LDO | 1.3V | 1.2.4 |
| DAC\_LOCAL\_BIAS\_A | 10uA | 1.2.5 |
| DAC\_LOCAL\_BIAS\_B | 10uA | 1.2.6 |
| ADC\_A\_REFP | 1.35v | 1.2.7 |
| ADC\_A\_REF\_CM | 1.1v | 1.2.8 |
| ADC\_A\_REFN | 0.85v | 1.2.9 |
| ADC\_B\_REFP | 1.35v | 1.2.10 |
| ADC\_B\_REF\_CM | 1.1v | 1.2.11 |
| ADC\_B\_REFN | 0.85v | 1.2.12 |
| ADC\_C\_REFP | 1.35v | 1.2.13 |
| ADC\_C\_REF\_CM | 1.1v | 1.2.14 |
| ADC\_C\_REFN | 0.85v | 1.2.15 |
| ADC\_D\_REFP | 1.35v | 1.2.16 |
| ADC\_D\_REF\_CM | 1.1v | 1.2.17 |
| ADC\_D\_REFN | 0.85v | 1.2.18 |
| DVDD\_LDO | 0.9V | 1.2.19 |
| SAR\_VREF\_1 | 0.9V | 1.2.20 |
| SAR\_VREF\_2 | 0.9V | 1.2.21 |
| SAR\_VREF\_3 | 0.9V | 1.2.22 |
|  |  |  |

TABLE 1.1

* 1. SPI configuration

#### 1.2.1 VBG Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR | 0x6063\_2014 | 0X0000\_0000 | set VBG output |

TABLE 1.2.1

#### 1.2.2 PMU\_IOUT Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR | 0x6063\_2014 | 0X0000\_000A | set EN\_VBG\_TEST=1 |

TABLE 1.2.2

#### 1.2.3 AVDDL\_LDO Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR | 0x6063\_20AC | 0x0000\_0008 | 1. enable AVDDL\_LDO test swich |
| WR | 0x6063\_2000 | 0x0000\_000C | 2. enable top AVDDL\_LDO test switch |

TABLE 1.2.3

#### 1.2.4 OSC\_LDO Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR | 0x6063\_2010 | 0x0000\_0020 | 1. enable OSC test switch |
| WR | 0x6063\_2000 | 0x0000\_001C | 2. enable top OSC test switch |

TABLE 1.2.4

#### 1.2.5 DAC\_LOCAL\_BIAS\_A Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR | 0x6063\_2000 | 0X0000\_0018 | analog test mux select DAC\_A |
| WR | 0x6068\_0384 | 0X0003\_0000 | select signal LOCAL\_BIAS\_CUR |

TABLE 1.2.5

#### 1.2.6 DAC\_LOCAL\_BIAS\_B Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR | 0x6063\_2000 | 0X0000\_0016 | analog test mux select DAC\_B |
| WR | 0x6068\_0388 | 0X0000\_0300 | select signal LOCAL\_BIAS\_CUR |

TABLE 1.2.6

#### 1.2.7 ADC\_A\_REFP Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR | 0x6063\_2000 | 0X0000\_0014 | select ADC A test |
| WR | 0x6068\_0390 | 0X0000\_8000 | mux ADC A REFP to test |

TABLE 1.2.7

#### 1.2.8 ADC\_A\_REF\_CM Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR | 0x6063\_2000 | 0X0000\_0014 | select ADC A test |
| WR | 0x6068\_0390 | 0X0000\_C000 | mux ADC A REF\_CM to test |

TABLE 1.2.8

#### 1.2.9 ADC\_A\_REFN Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR | 0x6063\_2000 | 0X0000\_0014 | select ADC A test |
| WR | 0x6068\_0390 | 0X0000\_A000 | mux ADC A REFN to test |

TABLE 1.2.9

#### 1.2.10 ADC\_B\_REFP Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR | 0x6063\_2000 | 0X0000\_0012 | select ADC B test |
| WR | 0x6068\_0394 | 0X0000\_0080 | mux ADC B REFP to test |

TABLE 1.2.10

#### 1.2.11 ADC\_B\_REF\_CM Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR | 0x6063\_2000 | 0X0000\_0012 | select ADC B test |
| WR | 0x6068\_0394 | 0X0000\_00C0 | mux ADC B REF\_CM to test |

TABLE 1.2.11

#### 1.2.12 ADC\_B\_REFN Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR | 0x6063\_2000 | 0X0000\_0012 | select ADC B test |
| WR | 0x6068\_0394 | 0X0000\_00A0 | mux ADC B REF\_CM to test |

TABLE 1.2.12

#### 1.2.13 ADC\_C\_REFP Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR | 0x6063\_2000 | 0X0000\_0010 | select ADC C test |
| WR | 0x6068\_0394 | 0X8000\_0000 | mux ADC C REF\_P to test |

TABLE 1.2.13

#### 1.2.14 ADC\_C\_REF\_CM Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR | 0x6063\_2000 | 0X0000\_0010 | select ADC C test |
| WR | 0x6068\_0394 | 0XC000\_0000 | mux ADC C REF\_CM to test |

TABLE 1.2.14

#### 1.2.15 ADC\_C\_REFN Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR | 0x6063\_2000 | 0X0000\_0010 | select ADC C test |
| WR | 0x6068\_0394 | 0XA000\_0000 | mux ADC C REF\_N to test |

TABLE 1.2.15

#### 1.2.16 ADC\_D\_REFP Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR | 0x6063\_2000 | 0X0000\_000E | select ADC D test |
| WR | 0x6068\_0398 | 0X0080\_0000 | mux ADC D REF\_P to test |

TABLE 1.2.16

#### 1.2.17 ADC\_D\_REF\_CM Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR | 0x6063\_2000 | 0X0000\_000E | select ADC D test |
| WR | 0x6068\_0398 | 0X00C0\_0000 | mux ADC D REF\_CM to test |

TABLE 1.2.17

#### 1.2.18 ADC\_D\_REFN Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR | 0x6063\_2000 | 0X0000\_000E | select ADC D test |
| WR | 0x6068\_0398 | 0X00A0\_0000 | mux ADC D REF\_N to test |

TABLE 1.2.18

#### 1.2.19 DVDD\_LDO Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR | 0X6063\_2114 | 0x0000\_0004 | 1. enable DVDD\_LDO test swich |
| WR | 0x6063\_2000 | 0x0000\_0026 | 2. enable top DVDD\_LDO test switch |

TABLE 1.2.19

#### 1.2.20 SAR\_VREF\_1 Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR | 0x6063\_2000 | 0X0000\_0024 | set SAR1\_TSTOUT to TOP\_TESTOUT\_MUX |
| WR | 0x6068\_0380 | 0X0005\_0000 | test SAR1\_VREF |

TABLE 1.2.20

#### 1.2.21 SAR\_VREF\_2 Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR | 0x6063\_2000 | 0X0000\_0022 | set SAR2\_TSTOUT to TOP\_TESTOUT\_MUX |
| WR | 0x6068\_0384 | 0X0000\_0005 | test SAR2\_VREF |

TABLE 1.2.21

#### 1.2.22 SAR\_VREF\_3 Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR | 0x6063\_2000 | 0X0000\_0020 | set SAR3\_TSTOUT to TOP\_TESTOUT\_MUX |
| WR | 0x6063\_2044 | 0X0000\_0005 | test SAR3\_VREF |

TABLE 1.2.22

1. PLL frequency test.

There are total 10 PLLs in Sirius: ADDAPLL, DSPPLL0, DSPPLL1, DSPPLL2, SDCPLL, AUPLL, PIXPLL, A7PLL, CEVAPLL and DDRPLL. The topology is shown in the figure below.



Fig 2.1 Sirius clock test diagram

### 2.1 PLL frequency test

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Pad Number | Pad Name | Signal Name | Value (MHz) | Tolerance (%) | Note |
|  | AD\_IN\_4 | SAR10\_IN\_3[4] | 20 | 1 | See 2.1.1  ADDAPLL CLKDIV 20MHz |
| 15.625 | 1 | See 2.1.2  DSPPLL0  2G/128=15.625M |
| 11.71875 | 1 | See 2.1.3  DSPPLL1  1.5G/128=11.71875M |
| 18.75 | 1 | See 2.1.4  DSPPLL2  2.4G/128=18.75M |
| 12.5 | 1 | See 2.1.5  SDCPLL  50M/4=12.5M |
| 5 | 1 | See 2.1.6  AUPLL  40M\*32/256=5M |
| 18.5625 | 2 | See 2.1.7  PIXPLL  74.25/4=18.5625MHz |
| EKB: QE0\_1 | DE1\_PAD | DE1 | 31.25 | 1 | See 2.1.8  A7PLL  500M/16=31.25M |
| EKB: QE0\_0 | PCLK1\_PAD | PCLK1 | 31.25 | 1 | See 2.1.9  CEVAPLL  500M/16=31.25M |
| EKB: I2S\_WS2 | QE1\_3\_PAD | QE1\_3 | 16.65625 | 2 | See 2.1.10  DDRPLL  533/32=16.65625MHz |

TABLE 2.1

* 1. SPI configuration
     1. ADDA PLL test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR | 0X6063\_2020 | 0x0000\_0002 | 1. enable ADDAPLL feedback clock test out |
| WR | 0x6063\_20B0 | 0x0000\_0010 | 2. set ABB TOP clock test mux |

TABLE 2.2.1

* + 1. DSPPLL0 test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR | 0X6063\_20B8 | 0x0000\_00C8 | 1. enable DSPPLL0 feedback clock test out |
| WR | 0x6063\_20B0 | 0x0000\_0011 | 2. set ABB TOP clock test mux |

TABLE 2.2.2

* + 1. DSPPLL1 PLL test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR | 0X6063\_20D0 | 0x0000\_0096 | 1. set DSPPLL1 vco freq to 1.5G |
| WR | 0x6063\_20B0 | 0x0000\_0012 | 2. set ABB TOP clock test mux |

TABLE 2.2.3

* + 1. DSPPLL2 test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR | 0X6063\_20E8 | 0x0000\_003C | 1. set DSPPLL2 vco freq to 2.4G |
| WR | 0x6063\_20B0 | 0x0000\_0013 | 2. set ABB TOP clock test mux |

TABLE 2.2.4

* + 1. SDCPLL test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR | 0X6063\_2104 | 0x0000\_003C | 1. set SDCPLL vco freq to 1.6G, post div=/128 |
| WR | 0x6063\_20FC | 0x0000\_0004 | 2. set SDCPLL EN\_TEST=1 |
| WR | 0x6063\_20B0 | 0X0000\_0014 | 3. set ABB TOP clock test mux |

TABLE 2.2.5

* + 1. AUPLL test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR | 0x6063\_2138 | 0X0000\_0020 | 1. set AUPLL loop div=32 |
| WR | 0x6063\_213C | 0X0000\_00C0 | 2. set AUPLL clkref sel mux; loopdiv sel mux |
| WR | 0x6063\_2140 | 0X0000\_00FE | 3. set AUPLL postdiv |
| WR | 0x6063\_2144 | 0X0000\_0081 | 4. set AUPLL postdiv(cont.); postdiv sel mux |
| WR | 0x6063\_2148 | 0X0000\_0007 | 5. set AUPLL test en, test sel |
| WR | 0x6063\_20B0 | 0X0000\_0016 | 6. set ABB TOP clock test mux |

TABLE 2.2.6

* + 1. PIXPLL test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR | 0x6063\_2A10 | 0x0563\_1FE4 | 1.set synthesizer output clock =400/5.3872=74.25MHz |
| WR | 0X6063\_212C | 0x0000\_0034 | 2. set pixpll loop divider=16, post divider=64,  output clock=74.25\*16/64=18.5625MHz |
| WR | 0x6063\_2124 | 0x0000\_0004 | 3. enable pixpll test clock out |
| WR | 0x6063\_20B0 | 0x0000\_0015 | 4. set ABB TOP clock test mux |

TABLE 2.2.7

* + 1. A7PLL test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR | 0x6061\_0000 | 0X0000\_3200 | 1. set A7PLL freq to 500M, default div 16 on SOC |
| R | 0x6061\_0004 | 0x0000\_0001 | 2. read A7PLL lock signal |

TABLE 2.2.8

* + 1. CEVAPLL test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR | 0x6457\_0000 | 0X0000\_3200 | 1. set CEVAPLL freq to 500M, default div 16 on SOC |
| R | 0x6457\_0004 | 0x0000\_0001 | 2. read CEVAPLL lock signal |

TABLE 2.2.9

* + 1. DDRPLL test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR | 0x6063\_2A00 | 0x0600\_F5E9 | 1. set synthesizer output clock=400/6.00375=66.625MHz |
| WR | 0x6456\_C004 | 0x0034\_0004 | 2. set loop divider=16, post divider=64, enable test clock,  test output clock=66.625\*16/64=16.65625MHz |

TABLE 2.2.10

1. DAC-ADC loop test

### 3.1 DAC-ADC loop test description

We will use the build-in sine-wave generator’s output as DAC’s 12bit input data. The DACs outputs will be a 2MHz single-tone sine waveform. And in load board we need to connect DAC’s output first to a filter whose -3dB corner is 10MHz, and filter order should be larger than 3th. Then filter output should pass a relay, relay’s one output could be connect to spectrum to observe DAC’s output spectrum. And the other output should connect to another relay. This relay can also select input from signal generator. The output connect to relay and finally to ADCA/ADCB or ADCC/ADCD. We have internal FFT processor to compute the ADC output ‘s SNR, THD, SNDR, and we can also mux one channel ADC’s output to monitor pin and use logic analyzer to analyze the data. The loop SNR should be >52dB.

Figure 3 shows the test bench for loop test.



Figure 3 Sirius DA/AD loop Test Bench

### 3.2 SPI configuration

Below table is for DA/AD loop test

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| WR/RD | Address | Reg Num | Data | Note |
| WR | 0x6068\_00C3[0] |  | 1’b1 |  |
| WR | 0x6068\_0191 |  | 0x0F | Select page one register |
| WR | 0x6068\_0192[1] |  | 1’b1 | debug sin wave output mode |
| WR | 0x6068\_0193[1] |  | 1’b0 | debug mode for single tone |
| WR | 0x6068\_0191[3] |  | 1’b1 | TX calibration off |
| WR | 0x6068\_0190[3:2] |  | 2’b01 | Single max tone gain-3db |
| WR | 0x6068\_0190[1] |  | 1’b1 | Fix calibration result |
| WR | 0x6068\_01B0~0x1BF |  | 0x00 | Calibration sin force |
| WR | 0x6068\_01B2[7:0] |  | 0xFF | Calibration cos force |
| WR | 0x6068\_01B8[7:0] |  | 0xFF |
| WR | 0x6068\_01AB~0x1A8 |  | 32’h01400000 | Output 976.56kHz sin wave |
|  |  |  | 32’h02800000 | Output 976.56\*2kHz sin wave |
|  |  |  | 32’h05000000 | Output 976.56\*4kHz sin wave |
|  |  |  | 32’h0C800000 | Output 976.56\*10kHz sin wave |
|  |  |  | 32’h19000000 | Output 976.56\*20kHz sin wave |
| WR | 0x6068\_0000[7:0] |  | 0x00->0x01->0x00 | Toggle, high level lasts >10ns |
| WR | 0x6068\_01FF[1:0] |  | 2’b00 | Force to TX mode |
| WR | 0x6068\_0101[7:0] |  | 0x01 | Change to RF\_8003s |
| WR | RF\_8003S\_65[7:0] |  | 0x40 |  |
| WR | RF\_8003S\_69[0] |  | 1’b0 |  |
| WR | 0x6068\_0029[7:0] |  | 8’h38 | [7:3]: the number of points used as signal power, eg: 00111 means sum +/-7 points around signal into signal power  [2:1]: adc\_sel  00:adca, 01:adcb, 10:adcc, 11:adcd  [0]: iq\_sel  0:I, 1:Q |
| WR | 0x6068\_002A[7:0] |  | 8’h29 | [7]: mux for read only register  [6]: choose clock phase for 100M clk  [5]: 1’b1: adc’s output is 1’s  1’b0: adc’s output is 2’s  [4:2]: For precision. 3’h2 is recommend, which also should be changed according to the input signal  [1]: pulse signal, toggle once means test once  [0]: level signal, should be 1’b1 when test adc |
| WR | 0x6068\_002A[7:0] |  | 8’h2B | Wait 10ns |
| WR | 0x6068\_002A[7:0] |  | 8’h29 |  |
| RO | 0x6068\_0517[7:0] |  | 8’h01 | ADC test done signal, when read 8’h01, begin to read below register |
| RO | 0x6068\_0507~0504 | [31:0] |  | Snr(dB)=10\*log10(read\_out\_dec) >50 |
| RO | 0x6068\_050b~0508 | [31:0] |  | Power swing(read\_out\_dec) > 2500 |

TABLE 3.2

### 3.3 DAC test requirements

The following table shows the DACs test output requirements.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| DAC test output requirements | | | | |
| Number | Name | Value | Tolerance (%) | Note |
| 1 | Peak-to-Peak output swing | 0.7V | 15 | Differential value |
| 3 | SNDR | >50db |  | fout=2MHz, differential |
| 4 | IQ swing mismatch | 0 | 9 | Refer to 3.5 |
| 5 | Output common-mode voltage | 0.9V | 15 | The common-mode voltage at each DAC outputs. |
| 6 | Output DC offset | <15mV |  | Differential dc value, use test 5 result to generate:  Vdc\_off=Vcm+-Vcm- |

TABLE 3.3

### 3.4 DAC Test Related Pins

|  |  |
| --- | --- |
| Pin Name | Test Value Expression |
| QDAC\_OUTN\_A | V1 |
| QDAC\_OUTP\_A | V2 |
| IDAC\_OUTP\_A | V3 |
| IDAC\_OUTN\_A | V4 |
| IDAC\_OUTN\_B | V15 |
| IDAC\_OUTP\_B | V16 |
| QDAC\_OUTP\_B | V17 |
| QDAC\_OUTN\_B | V18 |

TABLE 3.4

### 3.5 DAC test definition

|  |  |  |
| --- | --- | --- |
| Name | Expression | Definition |
| Peak-to-Peak output swing | Vpp\_Q\_A | Max(V2-V1­)-Min(V2-V1­) |
| Vpp\_I\_A | Max(V3-V4­)-Min(V3-V4­) |
| Vpp\_Q\_B | Max(V17-V18­)-Min(V17-V18­) |
| Vpp\_I\_B | Max(V16-V15­)-Min(V16-V15­) |
| IQ\_mismatch | MA | 1-Vpp\_I\_A/ Vpp\_Q\_A |
| MB | 1-Vpp\_I\_B/ Vpp\_Q\_B |

TABLE 3.5

### 3.6 ADC test requirements

The following table shows the ADC external input mode test requirement

|  |  |  |  |
| --- | --- | --- | --- |
| 12 bit ADC test input and output requirements | | | |
| Number | Name | Value | Tolerance (%) |
| 1 | Input frequency | 9MHz | 10 |
| 2 | Input signal common-mode voltage value | 0.9V | 10 |
| 3 | Input signal differential peak-to-peak voltage | 0.7V | 10 |
| 4 | ADC output code peak-to-peak swing(DEC) | 2500 | 15 |
| 5 | ADC output code SNDR | >56dB |  |

TABLE 3.6

For ADC test SPI config setting, please follow DA/AD loop test setting in section 3.2.

## 4 SAR ADC test

SAR1/SAR2/SAR3 is single-ended 10-bit ADC, whose sampling rate is 100/11MHz. The outputs are denoted as D0~D9, where D9 is the MSB and D0 is the LSB. This SAR ADC only can be tested in DC voltage input case, and output data be read in register.

### 4.1 SAR ADC test requirement

The following table shows the test input and output requirements for the 10-bit ADC.

|  |  |  |
| --- | --- | --- |
| Input dc voltage(V) | Output code | Tolerant |
| 0 | 0 | 0<=delta<=5 |
| 0.45 | 10’d256 | -7<=delta<=+7 |
| 0.9 | 10’d512 | -10<=delta<=0 |
| 0<=delta<=+10 |
| 1.35 | 10’d768 | -15<=delta<=+15 |
| 1.8 | 10’d1024 | -20<=delta<=0 |

### 4.2 SPI configuration

SARADC setting

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RO | Address | Data | Note |
| WR | 0x6063\_20A8[7:0] | SAR10\_1: 8’hC0  SAR10\_2: 8’hD0  SAR10\_3: 8’hE0 | [7:4]: 1100: mux SAR10\_1 data out  1101: mux SAR10\_2 data out  1110: mux SAR10\_3 data out |
| RO | {0x6063\_2164[1:0], 0x6063\_2160[7:0]} |  | SARADC output code |

## 5 TS test.

The calibration principle of Temperature Sensor (TS) is to find out the precise temperature drift (T\_os, see section 5.2), store it in effuse and then compensate it in software stage.

### 5.1 Load Board Requirement

To perform FT calibration, a commercial temperature sensor is required to place near the test site to provide reference temperature. For multi-Site load board design, the placement of commercial TSs are suggested to avoid cross heating, as Fig 5.1 shown.

Please use high accuracy commercial TS products such as **ADT7420/7320 (require I2C or SPI interface, see Appendix I)** for temperature reference.



Fig 5.1 Commercial TS placement suggestion in multi-site load board

### 5.2 TS test requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| TS test requirements | | | | |
| Number | Name | Value | Tolerance | Note |
| 1 | T\_os | 8 | 0-31 | DUT temperature offset, need to store into efuse |

### 5.2 TS test definition

|  |  |  |
| --- | --- | --- |
| Name | Expression | Definition |
| D\_avg |  | Mean value of TS code readouts |
| T\_ate | **T\_ate=0.4825\*D\_avg-77.7** | Calculate DUT temperature |
| T\_ext |  | Mean value of commercial TS temperature |
| T\_os | T\_os=T\_ate-T\_ext+16 | Offset of DUT, store T\_os into effuse[4:0]. (Please refer to OTP plan for specific bit location) |

### 5.3 FT procedure and SPI configuration

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
|  |  |  | Commercial TS on loadboard keep working |
| WR | 0x6063\_2000 | 0X0000\_0001 | set TS enable |
| R | 0x6063\_2910 |  | Wait 50us and readout TS\_DOUT09<8:0>, repeat 4 times and take average code as D\_avg.  Calculate **T\_ate=0.4825\*D\_avg-77.7** |
|  |  |  | Readout average commercial TS temperature (at least 4 times average), denoted as T\_ext;), T\_os=T\_ate-T\_ext+16 and store into effuse[4:0] (Please refer to OTP plan for specific bit location) |
|  |  |  | If T\_os<0 or T\_os > 31, mark this chip as failed chip and discard it. |
|  |  |  | Please also save total current on AVDD18 and DVDD (whole chip current during this IP test) in log file for leakage check. |

## 6 PVT sensor test

Directly read PVT sensor output 16bit code from SPI and compare to ideal code.

### 6.1 PVT sensor test requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| PVT sensor test requirements | | | | |
| Number | Name | Value | Tolerance | Note |
| 1 | Code\_PVT | 89 | 60-212 | PVT sensor code readout |

### 6.2 SPI configuration

#### 6.2.1 ABB inside PVT

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR | 0x6063\_20A8[7:0] | 8’h10 | Mux PVT code output |
| RO | 0x6063\_2161[7:0]~2160[7:0] | [15:0] | Read PVT output code |

#### 6.2.2 A7 PVT

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR | 0x6061\_0018[7:0] | 8’h02 | Enable pvt sensor |
| RO | 0x6061\_0015~0014 | [15:0] | Read PVT output code |

#### 6.2.3 CEVA PVT

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR | 0x6457\_0030[7:0] | 8’h02 | Enable pvt sensor |
| RO | 0x6457\_002D~002C | [15:0] | Read PVT output code |

#### 6.2.4 ISP PVT

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR | 0x6063\_2B00[7:0] | 8’h05 | Enable pvt sensor |
| RO | 0x6063\_2B05~2B04 | [15:0] | Read PVT output code |

#### 6.2.5 DDR PVT

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR | 0x6063\_2B00[7:0] | 8’h05 | Enable pvt sensor |
| RO | 0x6063\_2B07~2B06 | [15:0] | Read PVT output code |